What is claimed is:

1. A transmitting circuit comprising

a clock signal transmitting circuit for transmitting a clock signal through a first signal line;

a synchronization data generating circuit for generating synchronization data which represents a delimiter of serial data being transmitted of a predetermined unit length, and whose value changes two or more times in a predetermined time interval associated with the clock signal; and

a data transmitting circuit for superposing the generated synchronization data on each serial data of the unit length and for synchronizing the serial data with the clock signal and transmitting the serial data through a second signal line.

2. A transmitting circuit as set forth in claim 1, wherein, as said synchronization data, said synchronization data generating circuit generates a set of data including inverted data of the last data of said unit-length serial data, and the last data after the inverted data.

3. A transmitting circuit as set forth in claim 1, wherein, as said synchronization data, said synchronization data generating circuit generates data whose value changes two or more times in one cycle

of said clock signal.

4. A transmitting circuit as set forth in claim 3, wherein, when serial data synchronized with a clock signal is transmitted by said data transmitting circuit, as said synchronization data, said synchronization data generating circuit generates data whose value changes two or more times in one cycle of the clock signal.

5. A transmitting circuit as set forth in claim 3, wherein

when said synchronization data is superposed and transmitted by said data transmitting circuit, the cycle length of said clock signal is extended, and thereby said synchronization data generating circuit generates synchronization data whose value changes two or more times in the extended cycle of the clock signal; and

said clock signal transmitting circuit generates said clock signal of an extended cycle length when said synchronization data is superposed and transmitted.

6. A transmitting circuit as set forth in claim 1, wherein, as said synchronization data, said synchronization data generating circuit generates data whose value changes two or more times within a period in which the level of the clock signal is constant, that is, from a rising edge to a next falling

edge, or from a falling edge to a next rising edge of said clock signal.

7. A transmitting circuit as set forth in claim 6, wherein, when serial data synchronized with a clock signal is transmitted by said data transmitting circuit, as said synchronization data, said synchronization data generating circuit generates data whose value changes two or more times within said period in which the level of the clock signal is constant.

8. A transmitting circuit as set forth in claim 6, wherein

when said synchronization data is superposed and transmitted by said data transmitting circuit, the length of a constant level of said clock signal is extended, and thereby said synchronization data generating circuit generates synchronization data whose value changes two or more times in the extended period of a constant level of the clock signal; and

said clock signal transmitting circuit generates said clock signal of an extended length of a constant level when said synchronization data is superposed and transmitted.

9. A transmitting circuit as set forth in claim 1, further comprising a parallel-serial converting circuit for converting parallel data being transmitted to serial

data, wherein

said synchronization data generating circuit generates synchronization data representing a delimiter of the converted serial data of a predetermined unit length;

said data transmitting circuit transmits the converted serial data.

10. A method of transmission comprising steps of:

transmitting a clock signal through a first signal line;

generating synchronization data which represents a delimiter of serial data being transmitted of a predetermined unit length, and whose value changes two or more times in a predetermined time interval associated with the clock signal; and

superposing the generated synchronization data on each unit-length serial data, synchronizing the serial data with the clock signal and transmitting the serial data through a second signal line.

11. A receiving circuit comprising

a clock signal receiving circuit for receiving a clock signal transmitted through a first signal line;

a serial data receiving circuit for receiving serial data synchronized with the clock signal and transmitted through a second signal line;

a synchronization data detection circuit for detecting data from the received serial data and using the same as synchronization data, said data changing its value two or more times within a predetermined period associated with the received clock signal; and

a data processing circuit for detecting the predetermined unit length of the received serial data by using the detected synchronization data as a delimiter.

12. A receiving circuit as set forth in claim 11, wherein said data processing circuit converts said received serial data of said detected predetermined unit length to parallel data.

13. A receiving circuit as set forth in claim 11, wherein

when said synchronization data detection circuit detected a set of data including the first received serial data, inverted data of the first received serial data after that, and again the first received serial data after the inverted data, the inverted data and further the first data thereafter is used as said synchronization data; and

said data processing circuit detects data of a predetermined unit length with the first data as the last data of the received serial data of the predetermined unit length.

14. A receiving circuit as set forth in claim 11, wherein, as said synchronization data, said synchronization data detection circuit detects data whose value changes two or more times in a cycle of said clock signal.

15. A receiving circuit as set forth in claim 11, wherein, as said synchronization data, said synchronization data detection circuit detects data whose value changes two or more times within a period in which the level of said clock signal is constant, that is, from a rising edge to a next falling edge, or from a falling edge to a next rising edge of the clock signal.

16. A method of reception comprising the steps of:

receiving a clock signal transmitted through a first signal line;

receiving serial data synchronized with the clock signal and transmitted through a second signal line;

detecting data from the received serial data as synchronization data, said data changing its value two or more times within a predetermined period associated with the received clock signal; and

detecting the predetermined unit length of the received serial data by using the detected

synchronization data as a delimiter.

17. A data communication apparatus comprising

a transmitting circuit including

a clock signal transmitting circuit for transmitting a clock signal through a first signal line;

a synchronization data generating circuit for generating synchronization data which represents a delimiter of serial data being transmitted of a predetermined unit length, and whose value changes two or more times in a predetermined time interval associated with the clock signal; and

a data transmitting circuit for superposing the generated synchronization data on each serial data of the unit length and for synchronizing the serial data with the clock signal and transmitting the serial data, and

a receiving circuit including

a clock signal receiving circuit for receiving a clock signal transmitted through a first signal line;

a serial data receiving circuit for receiving serial data synchronized with the clock signal and transmitted through a second signal line;

a synchronization data detection circuit for detecting data from the received serial data as

synchronization data, said data changing its value two or more times within a predetermined period associated with the received clock signal; and

a data processing circuit for detecting the predetermined unit length of the received serial data as a delimiter of the detected synchronization data.

18. A data communication apparatus as set forth in claim 17, wherein

as said synchronization data, said synchronization data generating circuit of said transmitting circuit generates a set of data including inverted data of the last data of said unit-length serial data, and the last data after the inverted data, and

when said synchronization data detection circuit of said receiving circuit detected a set of data including the first received serial data, the inverted data of the first received serial data thereafter, and again the first received serial data after the inverted data, the inverted data and the first data thereafter is recognized as said synchronization data; and

said data processing circuit detects data of a predetermined unit length with the first data as the last data of the received serial data of the predetermined unit length.

19. A data communication apparatus as set forth in

claim 17, wherein

as said synchronization data, said synchronization data generating circuit of said transmitting circuit generates data whose value changes two or more times in one cycle of said clock signal.

as the synchronization data, said synchronization data detection circuit of said receiving circuit detects data whose value changes two or more times in one cycle of the clock signal.

20. A data communication apparatus as set forth in claim 19, wherein, when synchronized serial data is transmitted by said data transmitting circuit, as said synchronization data, said synchronization data generating circuit of said transmitting circuit generates data whose value changes two or more times in one cycle of a clock signal.

21. A data communication apparatus as set forth in claim 19, wherein,

when said synchronization data is superposed and transmitted by said data transmitting circuit, the cycle length of said clock signal is extended, and thereby said synchronization data generating circuit of said transmitting circuit generates synchronization data whose value changes two or more times in the extended cycle of the clock signal; and

said clock signal transmitting circuit of the transmitting circuit generates the clock signal of an extended cycle length when said synchronization data is superposed and transmitted.

22. A data communication apparatus as set forth in claim 17, wherein,

as said synchronization data, said synchronization data generating circuit of said transmitting circuit generates data whose value changes two or more times within a period in which the level of said clock signal is constant, that is, from a rising edge to a next falling edge, or from a falling edge to a next rising edge of the clock signal;

as said synchronization data, said synchronization data detection circuit of said receiving circuit detects data whose value changes two or more times within a period in which the level of said clock signal is constant, that is, from a rising edge to a next falling edge, or from a falling edge to a next rising edge of the clock signal.

23. A data communication apparatus as set forth in claim 22, wherein when synchronized serial data is transmitted by said data transmitting circuit, as said synchronization data, said synchronization data generating circuit of said transmitting circuit generates

data whose value changes two or more times within said period in which the level of a clock signal is constant.

24. A data communication apparatus as set forth in claim 22, wherein

when said synchronization data is superposed and transmitted by said data transmitting circuit, the length of a constant level of said clock signal is extended, and thereby said synchronization data generating circuit of the transmitting circuit generates synchronization data whose value changes two or more times in the extended cycle of the clock signal; and

said clock signal transmitting circuit of the transmitting circuit generates the clock signal of an extended length of a constant level when said synchronization data is superposed and transmitted.

25. A data communication apparatus as set forth in claim 17,

said transmitting circuit further comprising a parallel-serial converting circuit for converting parallel data being transmitted to serial data, wherein

said synchronization data generating circuit of the transmitting circuit generates synchronization data representing a delimiter of the converted serial data of a predetermined unit length;

said data transmitting circuit of the transmitting circuit transmits the converted serial data,

said data processing circuit of said receiving circuit converts said received serial data of said detected predetermined unit length to parallel data.